IT IS CLAIMED:

1. A method of operating a non-volatile memory, comprising:

utilizing a non-volatile memory with multiple planes each having a plurality of memory units comprising one or more blocks of memory cells sharing common word lines, wherein a block is the smallest erasable group of memory cells; and

avoiding the simultaneous programming of multiple units in a common plane while simultaneously programming a plurality of said units.

2. The method of claim 1, further comprising:

prior to said avoiding the simultaneous programming, receiving a request for the simultaneous programming of multiple ones of said memory units.

3. The method of claim 2, wherein said avoiding comprises:

comparing said multiple units to determine whether any of the multiple units belong to the same plane; and

programming the units that belong to the same plane in a time sequence.

4. The method of claim 2, further comprising:

prior to said receiving a request, establishing a maximum number of units to be programmed simultaneously, wherein said avoiding comprises establishing an order in which to program said maximum number of units to be programmed simultaneously.

5. The method of claim 4, wherein said avoiding further comprises:

subsequent to establishing the order, comparing said multiple units to determine whether any of the multiple units belong to the same plane; and

programming the units that belong to the same plane in a time sequence.

6. A method of operating a non-volatile memory, comprising:

utilizing an array of non-volatile memory cells, said array comprising a plurality of sub-arrays each having an independent set of word lines, wherein each of said sub-arrays is comprised of a plurality of independently programmable units, the units within a given sub-array having common word lines;

avoiding the simultaneous programming of units within the same sub-array while simultaneously programming a plurality of said units.

7. The method of claim 6, further comprising prior to said avoiding the simultaneous programming, receiving a request for the simultaneous programming of multiple ones of said units.

8. The method of claim 7, wherein said avoiding comprises:

comparing said multiple units to determine whether any of the multiple units form part of the same sub-array; and

programming the units that form part of the same sub-array in a time sequence.

9. The method of claim 7, further comprising prior to said receiving a request, establishing a maximum number of units to be programmed simultaneously, and wherein said avoiding comprises establishing an order in which to program said maximum number of units simultaneously to be programmed simultaneously.

10. The method of claim 9, wherein said avoiding comprises, subsequent to establishing a order:

comparing said multiple units to determine whether any of the multiple units form part of the same sub-array; and

programming the units that form part of the same sub-array in a time sequence.

11. A non-volatile memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of non-volatile memory cells each connected to a respective first bit line and a respective first word line, wherein information is stored in a given one of said cells by applying a first voltage to the respective first word line to which the given cell is connected and a second voltage to the respective first bit line to which the given cell is connected; and

a bit line driver connected to one or more of said bit lines, wherein the rate at which said bit line driver changes the voltage which it applies to a bit line to which it is connected is adjustable.

12. The non-volatile memory device of claim 11, wherein said rate is externally adjustable.

13. The non-volatile memory device of claim 11, further comprising:
a controller, wherein said rate is adjustable by the controller.

14. The non-volatile memory device of claim 13, wherein said controller adjusts said rate in response the amount of data error detected by the controller in the memory.

15. The non-volatile memory device of claim 13, wherein said controller adjusts said rate in a given sector of said memory based upon the number of times the given sector has been programmed.

16. The non-volatile memory device of claim 13, wherein said controller adjusts said rate in response the operating conditions of the memory.

17. The non-volatile memory device of claim 16, wherein the operating conditions include the temperature.

18. A method of operating a non-volatile memory, said non-volatile memory comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of non-volatile memory cells each connected to a respective first bit line and a respective first word line, wherein information is stored in a given one of said cells by applying a first voltage to the respective first word line to which the given cell is connected and a second voltage to the respective first bit line to which the given cell is connected; and

a bit line driver connected to one or more of said bit lines to apply a range of voltages;

the method comprising:

detecting one or more data errors in said non-volatile memory; and

altering the rate at which said bit line driver changes the voltage it is applying to a bit line to which it is connected in response to said detecting.

19. The method of claim 18, wherein said rate is set to an initial value by the manufacturer.

20. The method of claim 18, wherein said rate is altered externally.

21. The method of claim 18, said memory device further comprising:

a controller, wherein said rate is altered by the controller.

22. The method of claim 21, wherein said memory cells are divided into a number of sectors and wherein said rate is altered independently in each of said sectors.

23. The method of claim 22, wherein said memory cells are divided into a number of sectors and wherein said rate is altered independently in each of said sectors.

24. The method of claim 23, wherein said rate is altered in each of said sectors on a periodical basis.

25. The method of claim 24, wherein said periodic basis is determined by the number of times that the sector has been written.

26. In a non-volatile memory system including a plurality of bit lines oriented to cross a plurality of word lines with inductive coupling therebetween, a method of applying a voltage pulse to at least one selected bit line, comprising setting the rate of rise of said voltage pulse to control a level of current induced in at least one word line.

27. A method of operating a non-volatile memory, said non-volatile memory comprising:

a plurality of word lines;

a plurality of bit lines, at least some of the plurality of bit lines being inductively coupled with at least a group of the plurality of word lines; and

a plurality of non-volatile memory cells individually connected to at least one of the bit lines and to one of the word lines;

wherein data are simultaneously written into at least a given number of the plurality of cells that are connected to at least one selected of said group of word lines in a programming operation that applies a first voltage to the selected word line, a second voltage to at least some of the plurality of bit lines to which said given number of cells are connected, and a reference voltage to others of said group of word lines that are not selected;

said method comprising performing said programming operation by applying a pulse of the second voltage to at least some of the plurality of bit lines to which said given number of cells are connected in a manner to avoid disturbing data stored in those of the memory cells connected to said others of said word lines that are not selected.

28. The method of claim 27, wherein a ramp rate of a leading edge of said voltage pulse is selected to control the amount of voltage that is induced thereby into said others of the word lines that are not selected.

29. The method of claim 27, wherein a number of the plurality of bit lines receiving the pulse of the second voltage is less than those which could simultaneously receive said pulse to carry out the programming operation.